nigh-l', Superconductor-NorI~lal-Stlpcrcon(l~lctor Junctions with Polyimide-Passiv ated Ambient-Temperat u re Edge Formation

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Abstract **Superconducting-Normal-Superconductor (SNS) edge Josephson Junctions (JJ's) continue to be a focus of high-'I'$_c$ superconductor (11'1'S) electronics development, The abilitv to form clean edges in HTS materials is essential for successful SNS edge JJ's as well as crossovers and via contacts. We report a novel SNS JJ fabrication process in which a $YBa_2Cu_3O_{7-\delta}$ (YBLO) base electrode/$SrTiO_3$ (S'1'l)) insulator bilayer coated with a polyimide passivation layer is rotated during Ar ion milling through a reflowed photoresist mask to form omnidirectional edges. No sample cooling is used during milling. $YBa_2Cu_{2.8}Co_{0.2}O_{7-\delta}$ (YBCCO) normal layers and $Y1.a_{0.05}Ba_2Cu_3O_{7-\delta}$ (YBI .CO) counter-elect rodes completed the SNS JJ's. Devices fabricated using this polyimide passivation layer have significantly smaller standard deviations in critical current and resistance than those processed without it.**

1. INTRODUCTION

'1 he ability to control lably fabricate 11 igh-Temp erature Superconductor(] ITS) S-Normal-S (SNS) Josephson Junctions (JJ's) enhances the possibilities for many applications, including digital circuits, SQUID's, and mixers. A wide variety of approaches to fabricating SNS-like junctions has been tried and analyzed in terms of proximity effect behavior[I]. Since their initial successful demonstration[2], [3], most work has focused on SNS edge junctions for circuit applications. in Particular, edge SNS JJ's with normal Y11az(11$_2$79Co(, $_{21}O_{7-\delta}$ (YBCCO) inter] ayers [4]-[6] arc currently favored due to demonstrations of reproducible control of device parameters.

Very recently, 11'1'S SNS JJ's cm superconducting groundplanes were demonstrated [5], [6]. In order to assure successful fabrication of junctions on groundplanes, separate patterning of tbc groundplane and insulating oxide layers was eliminated. This minimized tbc number of layers exposed to photoresist/ion-milling processing and potential degradation of exposed surfaces and subsequently grown films due to processing residues. While this simplification allowed tbc very important demonstration of 11'1'S SNS JJ's on groundplanes, further improvements in tbc processing of edges arc needed in order to make this technology more flexible.

The use of polyimide films bas resulted in higher quality structures and cleaner surfaces in low-temperature superconducting materials processing[7], [8]. To this end, we investigated the use of a polyimide layer to reduce unwanted photoresist residues remaining after processing of oxide surfaces. in this work, we employed the edge SNS junction structure as a test vehicle to determine the relative merits of such a passivation scheme. We show that high-quality SNS devices can indeed be fabricated by including a polyimide passivation layer under tbc photoresist milling mask and that better control of the device parameters is achieved than in similarly fabricated devices fabricated without such a polyimide layer.

II. JUNCTION FABRICATION

A. Polyimide-Passivated Edge Junctions

SNS edge junction fabrication began with off-axis spotter deposition of $YBa_2Cu_3O_{7-\delta}$ (YBCO, 220 nm)/$SrTiO_3$ (STO, 300 nm) bilayers deposited onto 5 cm-diameter $LaAlO_3$ (1 00) wafers. Details of the deposition of these films were discussed previously [5] The transition temperature, determined by ac susceptibility, of the YBCO film was typically 86-87 K, with a width smaller than 1 K. The wafers were diced into 1 x1 and 0.5 x 0.5 cm^2 chips for processing into the SNS edge junctions. Prior to photolithogra phic processing, the chips were ultrasonically cleaned for 30 minutes in trichloroethylene, acetone and ethanol to remove any residues left by the dicing process. In addition, the chips were plasma cleaned in a reactive ion etch (RIE) system for 30 minutes at 120 W with 150 m'Torr 0_2.

The YBCO/STO bilayer was prebaked at 130^O C for onc minute to remove adsorbed water vapor anti coated with polyimide (CG285) spun at 5000 rpm for 40 seconds. The thickness of tbc polyimide layer was 500 nm. The polyimide-coated chip was partially cored at 130^O C for five minutes on a hot plate. After the chip was allowed to cool, a 1.5 µm thick layer of 1518 photoresist was spun onto the chip at 5000 rpm for 40 seconds and prebaked at 95^O C for 2 minutes. The

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resist edge bead was removed with a 3 minute exposure, development in AZ developer diluted 1:1 in water, rinse and drying, in dry N_2 gas. The exposure of the chips was performed with a 350 nm UV flax of 10 mW/cm^2 through chrome contact masks. The base-clectrodc pattern was then exposed for one minute and developed in the AZ (1:1) solution. The 1518 resist pattern was then baked at 130[] C for five minutes, hot enough to cause the edges of the mist to flow. Atomic Force Microscope (AFM) studies of the reflowed 1518 edges indicated that the edge angle, measured from the substrate plane, is -20° for line widths exceeding S pm.

The patterned chips were then mounted on a 1 mm-thick stainless-steel plate using Ag paint for milling using a 500 eV, 1mA/cm^2 Ar' ion beam at an angle 45^O from normal incidence. (Fig. 1). The plate was rotated at 35 rpm using a DC motor mounted in the vacuum system. Typically, 17 minutes was required to etch through the YBCO, S"1'0, and polyimide films; the total etching time was 20 minutes. Note that no cooling was provided to the sample during the entire ion-mill etch.

Following milling, the substrate was removed from the plate and excess Ag paint scrapped off of back. The sample was then placed in the RIE system for a 150 mTorr-O_2 plasma clean at 120 W for 30 minutes. This removed most of the cross-linked photoresist and polyimide. The sample was then ultrasonically cleaned in methylene chloride, acetone and ethanol for 10 minutes each. Methylene chloride is a solvent for polyimide CG285 and effectively lifts off any remaining moss-linked 1518 photoresist.

An AFM image of a YBCO/STO edge prepared with the polyimide-passivated reflowed resist is shown in Fig. 2, The edge is seen to be smooth and clear of large scale defects. The angles of the YBCO and STO portions of the edge arc 17^O and 10^O, respectively, from the plane of the substrate.. '1'here separate angles presumably result from differences in millings rate.

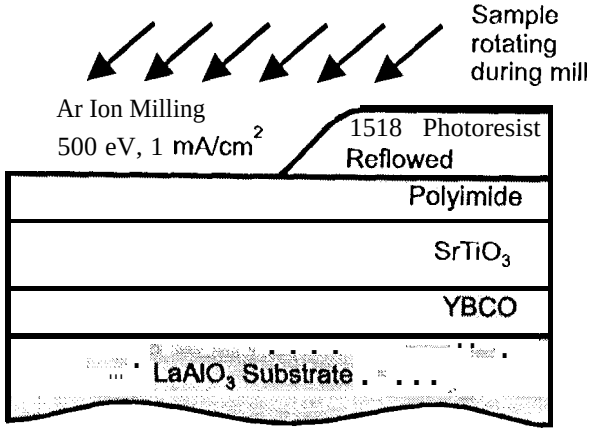

Fig. 1, - Cross section of the SNS edge junction structure during tapered edge formation. The polyimide passivation layer used below the reflowed-resist milling mask is unique to this wink. '1 he sample was not actively cooled during ion milling.

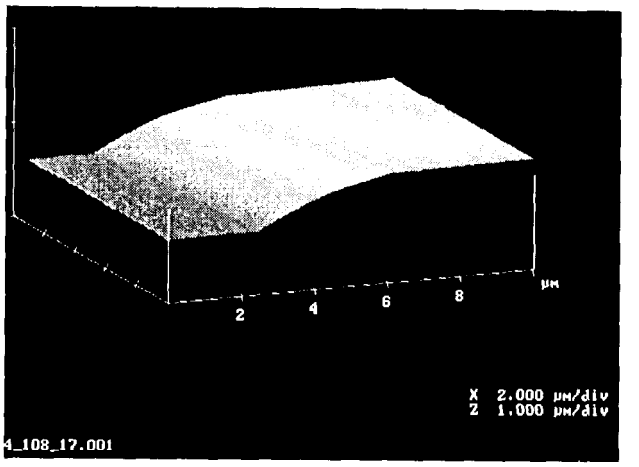

Fig ?. - AFM image of a YBCO/STO edge formed by milling, the bilayer film coated with a polyimide passivation layer using a rcfl{}}vcd-resist mask. The sample holder was rotated but not actively cooled during ion milling.

Following the edge formation step, the YBCCO normal interlayer, $YBa_{1.95}La_{0.05}Cu_3O_{7-\delta}$ (YBLCO) superconducting counterelectrode, and Au contact layer were deposited. The sample was mounted onto a Haines alloy plate with Ag paint and introduced into the load lock of a pulsed laser deposition (PLD) system containing a 5 cm-diameter ion source. 'l'he chip surface was spatter-cleaned in the load-lock chamber with a 100 eV, 1mA/cm^2 ion beam of Ar and O_2. The Ar partial pressure was 1.5x10^{-4}; total pressure was 2,0x 1 0^{-4} Torr. Etch time was five minutes, removing an estimated s nm of YBCO or STO.

The samples were then transferred *in situ* to the main deposition chamber. Prior to the deposition of the YBCCO N-layer ant! the YBLCO counterelectrode films, the substrate was heated to 820° C in 200 mTorr O_2 for 20 minutes. The YBCCO and YBLCO films were then deposited by P] ,1) (fluence of 1.6 J/cm^2 at λ= 248 rim). Substrate temperature was controlled by a thermocouple and measured with an optical pyrometer using heavily-doped Si chips mounted C1OSC to the device chips. During film deposition the laser spot was scanned over the 5 cm-diameter targets in a vertical direction and the substrate was oscillated ±1 cm in horizontal direction. This produced films with total thickness variation less than 10 % over a 1x1 cm^2 area. Following film deposition, the chip was cooled at 3^O C/rein, to room temperature in 500 Torr of 0_2. Following this anneal step, a 100 nm-thick Au film was deposited by dc spattering in 10 mTorr of Ar.

Edge SNS junction chips with YBCCO N-interlayer thicknesses of O, 10, 46 and 93 nm were fabricated, The YBLCO thickness was fixed at 200 nm. The YBCCO films had resistivities of 250 µΩ–cm at 60 K and transition temperatures of 45 K. The transition temperature of the YBLCO films were typically 88 K.

The chips were farther processed to define base-electrocIc contacts and to define the counter-electrode bridges. SNS

device widths were 1.25 - 10 pm. We have previously reported this part of the edge SNS device fabrication[9].

B. Edge Junctions without Polyimide Passivation

Control devices were also prepared without the polyimide passivation layer under the resist. 'lube same 1518 photoresist and base-cl ectrode patterning were used. } However, these chips were ion milled in an 10 cnl-diameter system with a water-coolecl, tiltable, rotating sample stage. Note that edges prepared with 1518 masks only and no water cooling were not acceptable for use in edge SNS devices. The chips were mounted on the sample stage with Ag grease. This system has a lower energy limit of 1000 eV, therefore the current density was lowered to <0.2 mA/cm^2 to reduce damage due to the higher ion energy. A milling time of 45 minutes was required to clear the chips to the substrate, Devices with YBCCO N interlayer thicknesses of O, 10, 20 and 30 nm were fabricated. The devices were completed with the process described above.

An AFM image ofa YBCO/STO edge produced with this 1 S 18 reflow process is shown in Fig. 3. The edge is smooth and clear of large scale defects, similar the edge shown in Fig. 2 produced by the polyimide passivation process. The YBCO edge angle of the edge is 13° from the plane of the substrate and the STO edge angle is 7^{O}. Notably different between the two AFM images (Figs. 2 and 3) is the smoothness outside of the area of the edge. The sample processed with the poly - imide passivation is smoother than the sample processed with only the reflowed resist. We farther note that subsequent Yll(X)-based layers grown on the chips processed with the polyimide passivation appear cleaner, by optical microscopy, than those without tbc passivation layer.

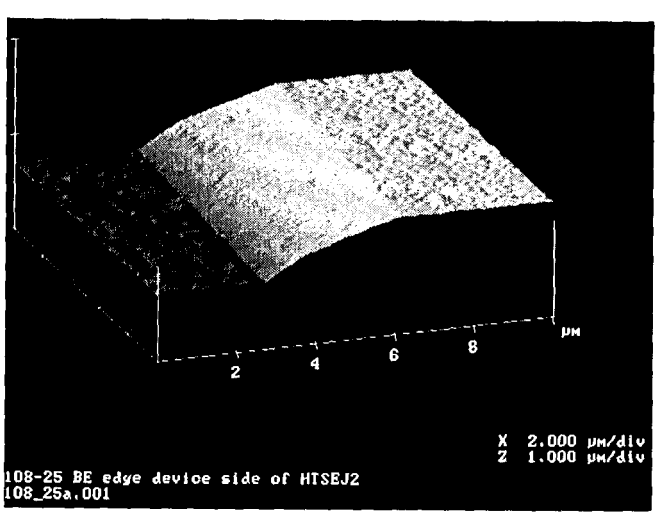

Fig 3. - AFM image of a YBCO/STO film edge formed by ion-milling with a ru(lc)wc.d-resist mask The sample stage was water cooled during ion milling Note the rougher surfaces than in Fig. 2.

111. ELECTRICAL MEASUREMENTS

Device chips were mounted in 28-pin ceramic chip packages and inserted into a magnetically shielded cryogenic probe equipped with a thermometer and resistive heater for DC measurements. The temperature was maintained by a controller. f:oar-wire measurements were performed with two Al wires ultrasonically bonded to the counter electrode of each device and two wires bonded to common base-electrode contacts, Current-voltage (IV) characteristics were obtained by current-biasing the devices using a audio function generator. The current, derived from a known series resistor, and the voltage signals from the device were fed into low-noise amplifiers, the outputs of which were fed into an analog-to-digital converter.

"l'he IV characteristics of a typical SNS edge JJ at 77 K, with and without microwave radiation, arc shown in Fig. 4. This device had a YBCCO interlayer thickness of 10 nm and was processed with the polyimide passivation layer. Similar IV characteristics were observed for junctions without the passivation layer. At 77 K, the critical-current density (J_c) of this device was 1.03x 104 A/cm^2, the resistance was 0.26 Ω, and the critical current-resistance (I_cR_n) product was 48 μV. The shape of the IV characteristic is qualitatively consistent with the resistively-shunted junction (RSJ) model with a small excess current. Well-clcfincd Shapiro steps arc evident under microwave irradiation.

For all devices fabricated, J_c was observed to decrease exponentially with increasing YBCCO thickness. For a given YBCCO thickness J_c was generally larger in devices fabricated with the polyimide passivation than in devices without it. Note, however, that the resistances of devices fabricated with the polyimide process were lower by about a factor of three than those of the devices fabricated with the reflowed resist mask alone, although all resistances were significantly higher than expected from YBCCO resistivity. This suggests a boundary or interface resistance in series with the normal interlayer. For YBCCO thicknesses of 10 nm, I_cR_n values of

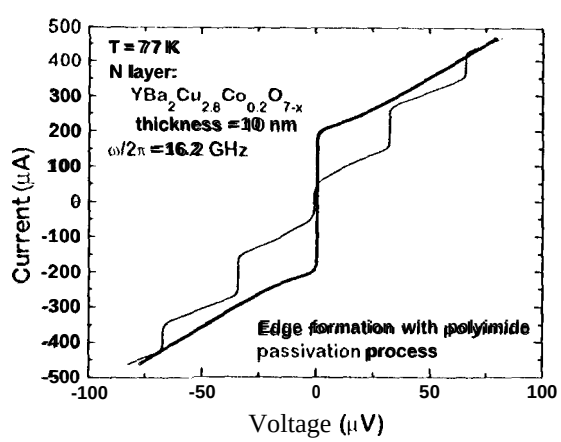

Fig 4. - IV characteristics of an SNS device fabricated with the polyimide passivation process. The data were taken at 77 K.

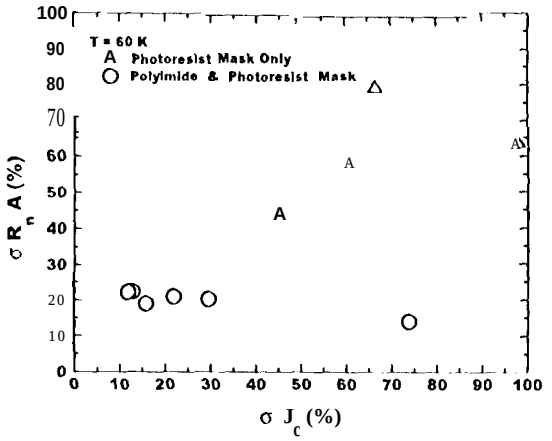

Fig. 5. - Device parameter spreads for each fabricated chip, with and without the polyimide passivation layer. The improved era-chip control with the polyimide process is clearly visible, The data were taken at 60 K and represent one standard deviation divided by the mean value expressed in percent

150 - 800 μV were observed at 60K independent of the method used to fabricate tbc edge.

The most significant difference between the two processes is shown in Fig. 5, in which the on-chip spread in R_nA (1 σ) is plotted against the spread in J_c. The data were taken at 60 K. All data from ten devices measured cm each fabricated chip are included. Clearly, device parameter spreads arc more tightly controlled in the polyimide process than in tbc simple reflow process. Note that the 74°/0 spread in J_c for the 93 nm-thick YBCCO polyimide-passivated chip is accounted for by tbc fact that the devices were just beginning to show an observable critical current at the measurement temperature. At 50 K, 1σ for J_c was 24%.

IV. CONCLUSION

Wc have fabricated SNS edge JJ's using a polyimide passivation layer underneath a reflowed-resist mask without actively cooling the chips during the ion-mill etch. This process produces devices with excellent IV characteristics and I_cR_n values as high as 800 μV at 60K. Compared with chips fabricated without the passivation layer on-chip device parameter spreads were significantly reduced by the new process.

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